1. AGENCY USE ONLY *(Leave blank)*	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	May 1994	Professional Paper

4. TITLE AND SUBTITLE
MOCVD GROWN SI-DOPED n^+InP LAYERS FOR THE SUBCOLLECTOR REGION IN HBTS

5. FUNDING NUMBERS
PR: EEB3
WU: DN304100

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8. PERFORMING ORGANIZATION REPORT NUMBER

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10. SPONSORING/MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION/AVAILABILITY STATEMENT

Approved for public release; distribution is unlimited.

13. ABSTRACT *(Maximum 200 words)*

This paper describes MOCVD Grown Si-Doped n^+InP Layers for the Subcollector Region in HBTs.

Subcollector layers in emitter-up HBTs are used to make ohmic contact to the collector region grown immediately above it. Ideally, the n^+ subcollector layer should have low electrical resistivity, good morphology and an abrupt high/low doping transition between it and the adjacent undoped collector region. Carrier concentrations in excess of $1x10^{19}/cm^3$ are desirable for low resistance contacts to the subcollector layers. Doping above $1x10^{19}/cm^3$ is reported for Sn (1,2),S,Se and Te dopants(3,4), but memory effects (i.e., continuing of the dopant incorporation into subsequently grown undoped layers) limit their usefulness. Si-doping of InP shows no memory problem (3,4), however maximum carrier concentrations seem to be limited to $<1x10^{19}/cm^3$, similar to Si-doped GaAs (5), above which degraded morphology occurs. Prospects for higher Si dopant saturation levels are seen from a few citations of carrier concentrations up to $\sim 2x10^{19}/cm^3$ (6,7) and some of these results suggest that lower growth temperature may be the key to achieving higher Si-doping.

Published in Proceedings of the *InP and Related Materials Conference*, 1994.

14. SUBJECT TERMS	15. NUMBER OF PAGES
electronic devices ion beam technology VLSI/VH	16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	SAME AS REPORT

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MP8

MOCVD Grown Si-Doped n^+ InP Layers for the Subcollector Region in HBTs

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Introduction

Subcollector layers in emitter-up HBTs are used to make ohmic contact to the collector region grown immediately above it. Ideally the n^+ subcollector layer should have low electrical resistivity, good morphology and an abrupt high/low doping transition between it and the adjacent undoped collector region. Carrier concentrations in excess of $1x10^{19}/cm^3$ are desirable for low resistance contacts to the subcollector layers. Doping above $1x10^{19}/cm^3$ is reported for Sn (1,2), S, Se and Te dopants(3,4), but memory effects (i.e., continuing of the dopant incorporation into subsequently grown undoped layers) limit their usefulness. Si-doping of InP shows no memory problem (3,4), however maximum carrier concentrations seem to be limited to $< 1x10^{19}/cm^3$, similar to Si-doped GaAs (5), above which degraded morphology occurs. Prospects for higher Si dopant saturation levels are seen from a few citations of carrier concentrations up to $\sim 2x10^{19}/cm^3$ (6,7) and some of these results suggest that lower growth temperature may be the key to achieving higher Si-doping.

Experimental

To explore the possibilities of achieving higher n-type doping with Si, we have done a systematic assessment of Si-doping dependence on growth conditions. In a previous work (4), we have categorized the dependence of moderate silicon doping ($n \leq 1x10^{18}/cm^3$) of InP on growth conditions, which is summarized in Table 1. The growth conditions which produced the highest concentrations were used as a starting point for this study.

Table 1: Dependence of carrier concentration of InP:Si for moderate doping concentrations (Ref 4)

Growth Parameter	Carrier Concentration Dependency
Growth Pressure (Constant silane flow)	Linearly proportional
Growth Temperature	Increases, doubling from 550°C to 700°C
Silane flow	Linearly proportional
Trimethylindium flow	Inversely proportional
Phosphine flow	Independent

The MOCVD growth was performed in a horizontal reactor with 100 sccm TMI flow (17°C bubbler temperature, 800 Torr bubbler pressure; concentration $\sim 8.3x10^{-5}$ m.f.), 200 sccm 10% PH_3 flow (concentration $\sim 1.33x10^{-2}$ m.f.), 1500 sccm total gas flow, with growth rates ~4 Å/sec. The dopant gas was 0.5 % silane in hydrogen (concentration ~ 3.3×10^{-6} m.f. per sccm). InP(Si) MOCVD growths were performed over a range of chamber pressures of 9 to 100 Torr and a temperatures range of 475°C to 650 °C.

The dependences of conductivity, σ, and carrier concentration, n, from Van der Pauw / Hall measurements, and of the morphology were characterized for InP(Si) at two growth temperatures (Tg), 550°C and 650°C, and at two growth pressures (Pg), 20 Torr and 100 Torr. The visual appearance of the layers is qualitatively described as either *smooth* (the layer looks shiny with quality similar to undoped InP), *textured* (the layer looks shiny but hazy), or *matte* (the layer looks dull grey matte). High magnification Nomarski micrographs show detail of the layer surfaces for the different regions. For the application as a low loss contact layer we have chosen to show the electrical data as the conductivity, σ, and the Hall effect free carrier concentration, n, since these should track each other as $\sigma = ne\mu$ (where e is the electron charge and μ the electron mobility).

Figure 1 shows the effect of Si-doping at high growth temperature and low pressure (Tg=650°C/Pg=20 Torr) for change of silane flows during MOCVD InP growths. The layer morphologies remain smooth up to carrier concentration of ~ 1×10^{19} cm^{-3}. At higher n it is evident that much of the additional Si incorporation is non-electrically active, and the degradation of the morphology suggests that precipitates of si disrupt the planar epilayer growth. At the onset of degraded morphology the carrier concentration initially saturates then continues to increase, while the conductivity decreases continuously.

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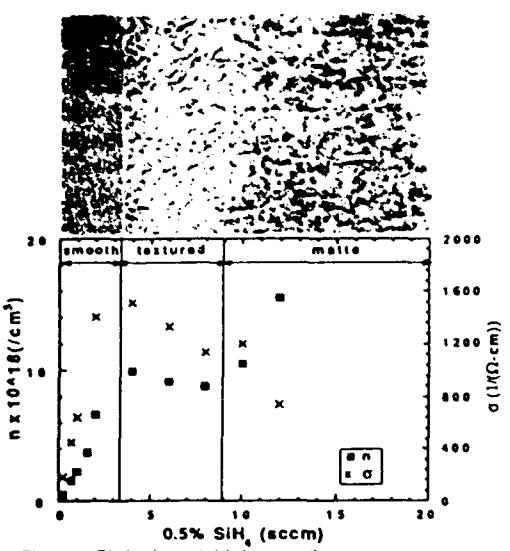

Fig. 1: Si-doping at high temp/low pressure (650°C/20 Torr)

The results for growth at high growth temperature/high pressure (Tg=650°C/Pg=100 Torr) shown in figure 2 are similar, however the morphology degradation makes a more abrupt transition from smooth to matte around $1x10^{19}/cm^3$. In this case σ simply saturates, even though n continues to increase. As expected the silane concentrations for comparable carrier concentrations are lower for the higher growth pressure.

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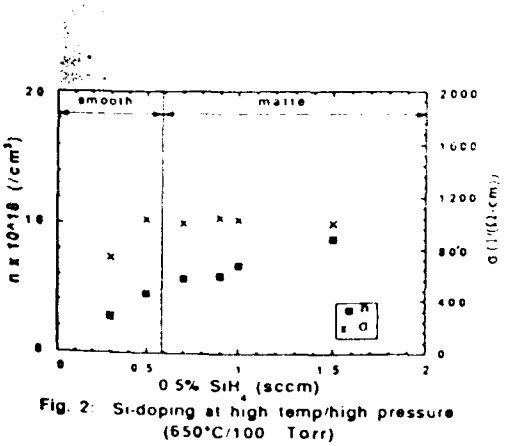

Fig. 2: Si-doping at high temp/high pressure (650°C/100 Torr)

Decrease of growth temperature to 550°C shows a significant increase in the achievable InP conductivity. For Si-doping at low growth temperature/low pressure (Tg=550°C/Pg=20 Torr) in figure 3 both σ and n increase with silane flow up to $n = 2.6 \times 10^{19}/cm^3$ at the maximum silane flow of 140 sccm. The combination of low temperature - low pressure severely reduces the Si incorporation efficiency, thus requiring excessive amount of silane. The excessive silane may limit the practicality of growing at lower temperatures. It is noteworthy that even with mole fractions of silane that exceed the TMI concentration by a factor of 5, there is no observable change in InP growth rate. There is little or no dependence of either the gas phase or surface InP growth chemistry on the presence of silane.

>10μm<

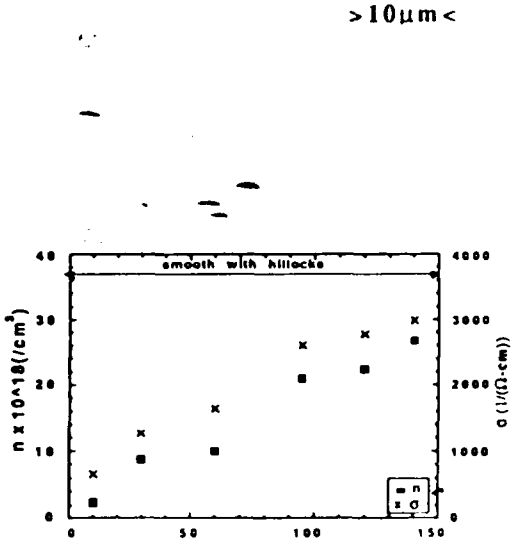

Fig. 3: Si-doping at low temp/low pressure (550°C/20 Torr)

For growth at 550°C - 100 Torr in figure 4, the greater Si-incorporation efficiency increases the range of Si to show saturation of n at ~ $2.6 \times 10^{19}/cm^3$ and degradation of the morphology for higher silane flow

>10μm<

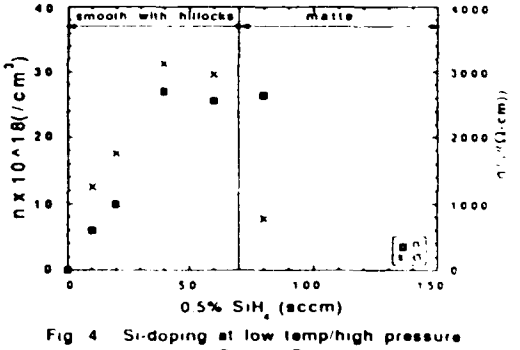

Fig 4 Si-doping at low temp/high pressure (550°C/100 Torr)

A new morphological problem, hillocks, is encountered for growths at 550°C . The formation of hillocks at these growth temperatures is not related to silicon doping, but appears to be related to substrate defects. The behavior of hillocks in InP MOCVD growth has been discussed recently by Nakamura (8), and their description is consistent with our own observations. The hillocks are believed to result from threading dislocations propagating from the substrate defects, thus the layer morphologies depend on the substrate quality and preparation. Inhibition of hillock formation can be achieved with higher growth temperatures or with higher growth rates - conditions which are counter to achieving high level Si incorporation. It is reported that for both InP(8) and GaAs (9,10) MOCVD growth, the hillock formation is inhibited with slight misorientation of the substrate from (100), thus the serious morphology problem from the 550°C growth may be avoidable.

At a constant temperature and pressure, a reduced TMI flow (and correspondingly reduced growth rate) increases the silicon incorporation, apparent in Table 2 . For both pairs of layers listed the increased carrier concentrations, as the TMI is reduced, are accompanied by morphology transition from shiny to dull grey matte.

Table 2: Effect of reduced TMI on InP(Si) layers

SiH_4 (sccm)	P (Torr)	SiH_4 (sccm)	TMI (sccm)	n, $x10^{18}$ (cm^{-3})	μ (cm^2/V-s)	morph -ology
20	9	20	100	5.5	1117	shiny
20	9	20	50	12	290	matte
40	9	40	100	7.6	1121	shiny
40	9	40	50	15	600	matte

The abruptness of high/low doping junctions was characterized using C-V measurements made with an electrochemical C-V profiler, PN4200 by Biorad. The measurements were made on samples with nominally 1 μm of undoped InP grown on top of 0.5 μm of heavily doped InP (Si) on a conductive InP (S) substrate. The carrier concentration on the highest doped samples (550 °C, 100 Torr) changed three orders of magnitude, $2x10^{16}/cm^3$ to $1.7x10^{19}/cm^3$, within 0.1 μm as shown in figure 5. The initial surface depletion is large, 0.7 μm, corresponding to a carrier concentration of $\sim 2x10^{15}/cm^2$. Subsequent growth of undoped InP layer showed background carrier concentration indicative of undoped material. High/low junctions were also grown using Sn, with similar carrier concentration levels, and characterized as shown in figure 6. They also show a fairly abrupt transition between the high/low region, but about an order of magnitude higher background carrier concentration remains within the undoped region. The initial surface depletion is much less, 0.2 μm, corresponding to a carrier concentration of $1.5x10^{16}/cm^3$. Subsequent growth of a thick InP layer shows a carrier concentration spike at the epi-layer/substrate interface, and a higher than usual background concentration which is larger near the epi-layer/substrate interface and tapers down toward the surface.

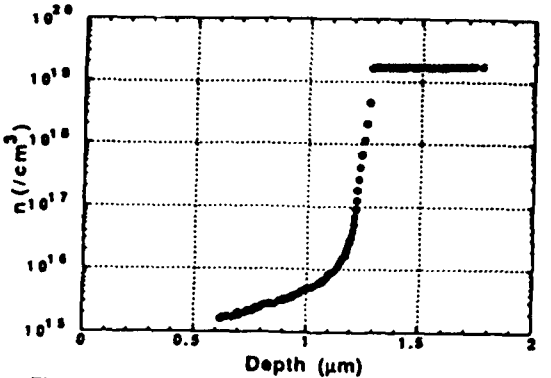

Fig. 5: Low/high junction InP (Si) measured by electrochemical C-V. n+ layer grown at 550°C, 20 Torr.

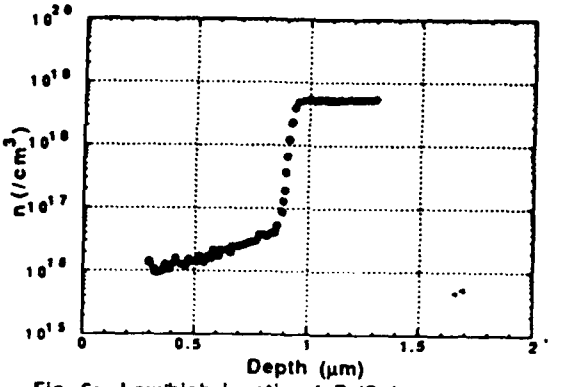

Fig. 6: Low/high junction InP (Sn) measured by electrochemical C-V. n+ layer grown at 650°C, 100 Torr.

Discussion

From the observed carrier concentration dependence on growth conditions, we believe that the limiting matte morphology of high silicon doped InP by MOCVD very likely results from the formation of Si precipitates. Our best results (highest doping with good morphology) occur for growth conditions which suppresses the time which silicon atoms have to migrate and find each other. Conditions which would allow clustering of the Si are those that would enhance Si surface diffusion such as high growth temperature and low growth rate. Our 650°C growth conditions seem to meet the conditions for easy Si migration and thus cause the rather low apparent solid saturation level of Si in InP. When the growth temperature is sufficiently low the Si atoms may be trapped on the surface due to their limited opportunity to migrate and thus become incorporated as electrically active donors in the lattice rather than forming neutral clusters. The prediction for MOCVD has been that growth temperatures are too high to observe this behavior(5) whereas it may be observable with the lower growth temperatures of MBE. In our case at 550°C we seem to be seeing this effect with the apparent higher Si solid saturation level at lower growth temperature.

The electrical behavior of the high Si doped layers also lends support that at high concentrations Si atoms cluster to form second phase precipitate inclusions in the InP layer. Charge carrier scattering from such inclusions would account for the reduced mobility. Wieder(11) discusses the effects of a second phase included in polycrystalline semiconductor layers and points out that the resulting change in n from measured Hall coefficients is small but that the change in measured conductivity is large, and this is the behavior we observe for InP(Si). Reduced mobility might also be explained by compensation, such as Si incorporation on P lattice sites or by interstitial Si/defect complexes to introduce electrical compensation. However studies correlating n to the amount of incorporated dopant for S(12) and for Sn(13), which show the same μ vs. n behavior as Si, also show no evidence that the dopant goes anywhere but on In lattice sites.

A possible interpretation of the cause of the matte morphology is that it to be related to a homogeneous gas phase reaction that forms solid particles that then disturb the epilayer growth. However the data of Table II indicate that gas phase reactions have not changed significantly. The silane flow is unchanged, thus there should be no increase in gas phase supersaturation to promote particle generation. Yet the matte morphology is observed when the TMI, and consequently the growth rate, is reduced. The higher n with the lower growth rate promotes formation of Si precipitates.

Conclusions

Carrier concentration levels up to $2.6 \times 10^{19}/cm^3$ from Si-doping of InP can be achieved with MOCVD by lowering growth temperature to 550°C. Formation of hillocks at this temperature (unrelated to the doping) limits the surface smoothness for device structures. However, reported use of off-orientation substrates to inhibit hillock formation offers an approach to take advantage of high levels of Si-doping for n+ InP grown at 550°C. Si-dopant is confirmed to show no evidence of memory effect for contaminating subsequently grown undoped InP in high/low doped structures.

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